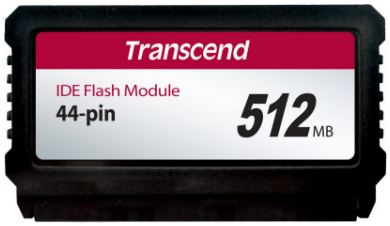
PTM520 / PTM720 / PTM820
IDE Flash Module

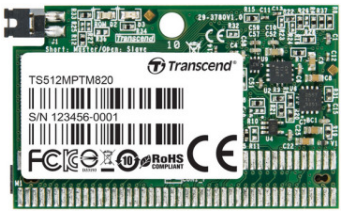
With an IDE interface and strong data retention ability, IDE Flash Modules are ideal for use in harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

40 Pin (Vertical)

44 Pin (Vertical)



44 Pin (Horizontal)



■ Features

- CE, FCC and BSMI compliance
- RoHS compliance
- Power supply: 3.3V/5V ±5%
- Operating temperature: 0ºC to 70ºC
- Storage temperature: -40ºC to 85ºC
- Humidity (Non condensation): 0% to 95%
- Built-in 72 bit per 1K Byte ECC (Error Correction Code) functionality to ensure high reliability of data transfer
- Global wear-leveling algorithm to eliminate excessive write operation and extend product life
- Supports S.M.A.R.T (Self-defined)
- Supports Security Command
- Supports Host Protected Area
- Supports Ultra DMA Mode 0 to 5
- Supports Multiword DMA Mode 0 to 2
- Supports PIO Mode 0 to 4
- Durability of connector: 100 times
- MTBF: 1,000,000 hours (in 25˚C)

■ Specifications

Physical Specification				
Part Number		PTM520	PTM720	PTM820
Form Factor		IDE Flash Module	IDE Flash Module	IDE Flash Module
Storage Capacity		128 MB to 4 GB	128 MB to 4 GB	128 MB to 4 GB
Dimensions (mm)	**Length**	61.0 ± 0.4	52.0 ± 0.40	45.0 ± 0.40
	Width	27.1 ± 0.50	29.5 ± 0.50	28.0 ± 0.20
	Height	7.1 ± 0.20	7.1 ± 0.20	6.0 ± 0.50
Input Voltage		3.3V/5V ± 5%	3.3V/5V ± 5%	3.3V/5V ± 5%
Weight		20g	20g	11g
Connector		40 pin IDE female	44 pin IDE female	44 pin IDE female

Environmental Specifications		
Operating Temperature		0 ℃ to 70 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Performance				
Model P/N	**Read (MB/s)**	**Write (MB/s)**	**Random Read (4KB QD32) (MB/s)**	**Random Write (4KB QD32) (MB/s)**
TS128MPTMX20	39.40	8.615	10.60	0.178
TS256MPTMX20	39.40	8.657	10.19	0.182
TS512MPTMX20	20.80	7.637	8.139	0.338
TS1GPTMX20	20.85	13.75	6.382	0.237
TS2GPTMX20	20.60	22.45	6.308	1.091
TS4GPTMX20	39.10	42.08	9.278	1.279

Note: 25 ℃, test on GA-Z87-UD3H-CF, 4GB RAM, Windows® 8.1 with AHCI mode, benchmark utility Crystal Disk Mark (version 3.0), copied file 1000MB.

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS128MPTMX20	249,984	248	16	63
TS256MPTMX20	499,968	496	16	63
TS512MPTMX20	1,000,944	993	16	63
TS1GPTMX20	1,957,536	1,942	16	63
TS2GPTMX20	3,915,072	3,884	16	63
TS4GPTMX20	7,831,152	7769	16	63

Power Consumption			
Input Voltage		5V ± 5%	3.3V ± 5%
Model P/N / Power Consumption		**Average (mA)**	**Average (mA)**
TS128MPTMX20	**Max Read**	99	99
	Max Write	85	85
	Idle	0.85	0.75
TS256MPTMX20	**Max Read**	98	98
	Max Write	84	84
	Idle	0.85	0.75
TS512MPTMX20	**Max Read**	75	75
	Max Write	70	69
	Idle	0.85	0.75
TS1GPTMX20	**Max Read**	77	77
	Max Write	87	86
	Idle	0.85	0.75
TS2GPTMX20	**Max Read**	80	80
	Max Write	109	109
	Idle	0.85	0.75
TS4GPTMX20	**Max Read**	108	108
	Max Write	161	159
	Idle	0.85	0.75

1. Tested with IOmeter running sequential reads/writes and idle mode.
2. StandBy Current : 5V : 2.8mA 3.3V : 2.2mA
3. All data above are maximum value of each measurement.

Reliability		
Data Reliability	Supports BCH ECC 72 bit per 1K byte	
Connector Durability	100 times	
MTBF	1,000,000 hours	
Endurance (TeraBytes Written)*	128MB	1.3 TB
	256MB	2.6 TB
	512MB	5.2 TB
	1GB	10.4 TB
	2GB	20.8 TB
	4GB	41.6 TB

*Note: Based on JEDEC JESD218A & 219A standard, Client Application Class with the following scenario: Active use: 40℃, 8hrs/day; Retention use: 30℃

Vibration	
Operating	3.0G, 5 - 800Hz
Non-Operating	5.0G, 5 - 800Hz

Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

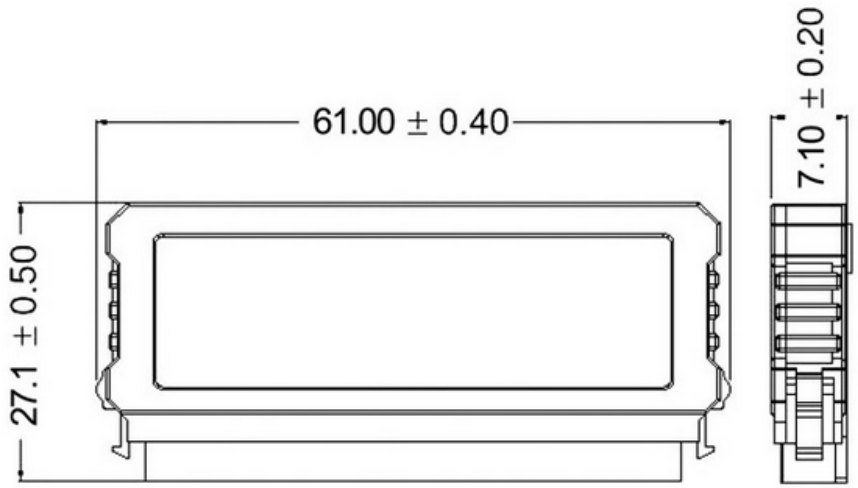
Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500G, 0.5ms, 3 times/dir., total 18 times.

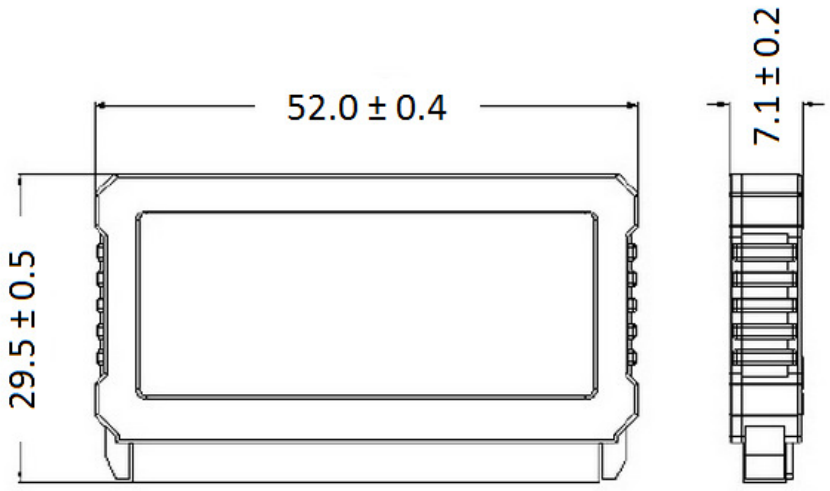
Regulations	
Compliance	CE, FCC and BSMI

Package Dimensions

The figure below illustrates the Transcend 40-Pin IDE Flash Module (**PTM520)** product. All dimensions are in mm.

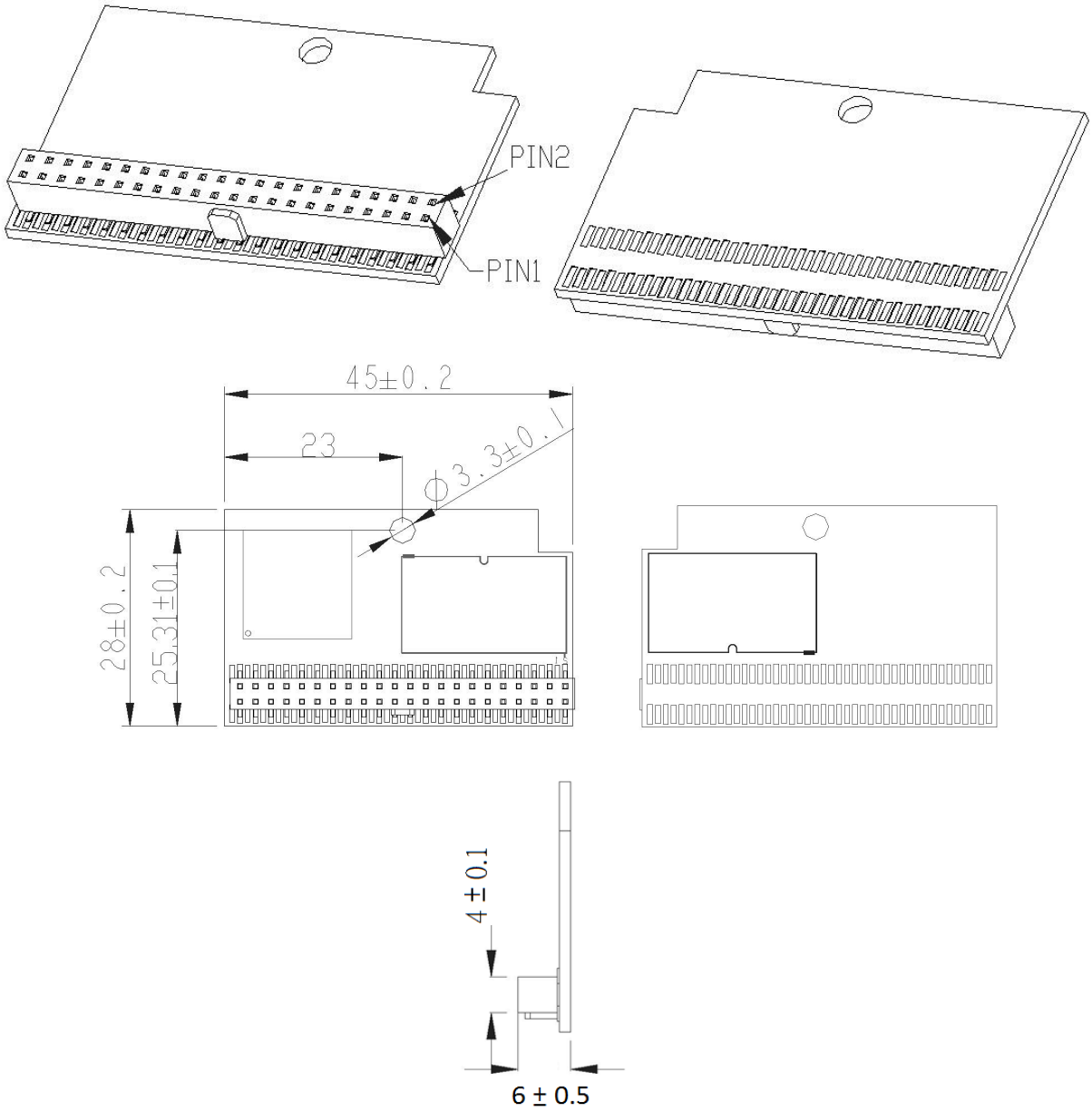


The figure below illustrates the Transcend 44-Pin IDE Flash Module (**PTM720)** product. All dimensions are in mm.

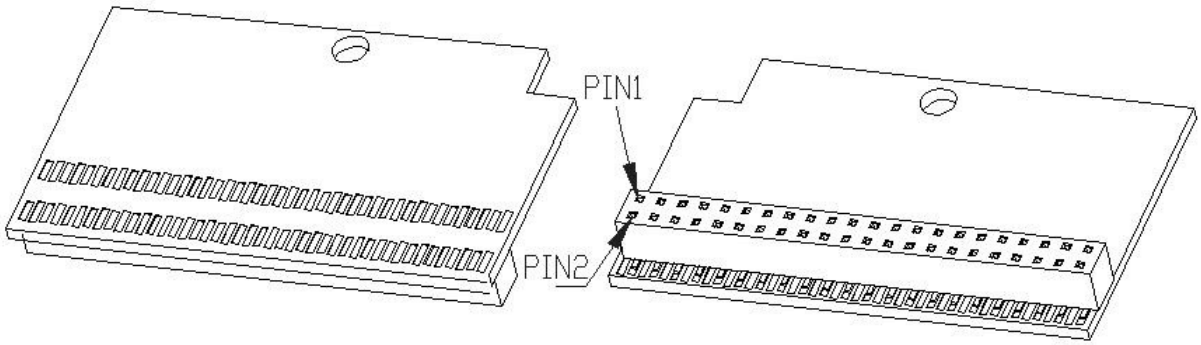


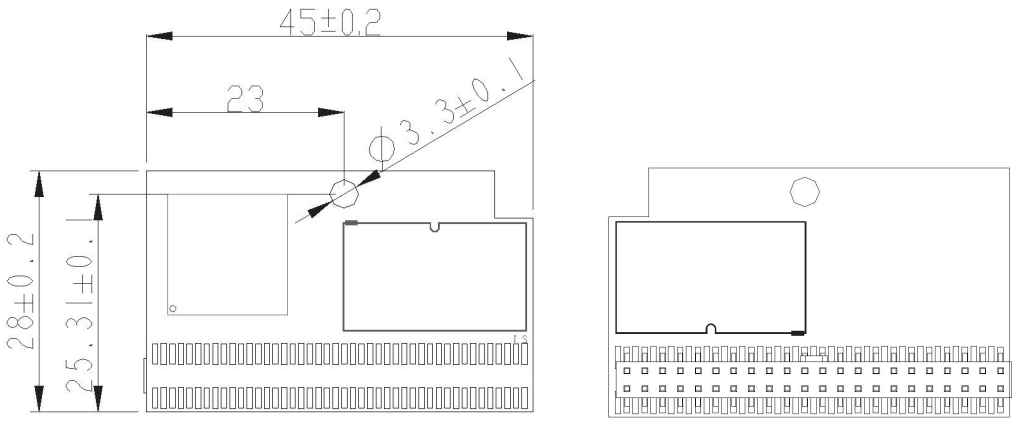
Below figure illustrates the Transcend 44-Pin IDE Flash Module (Horizontal) (**PTM820)**. All dimensions are in mm.

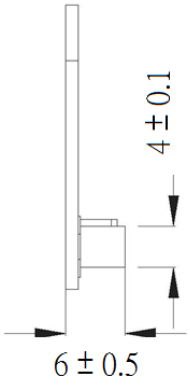
TYPE_1



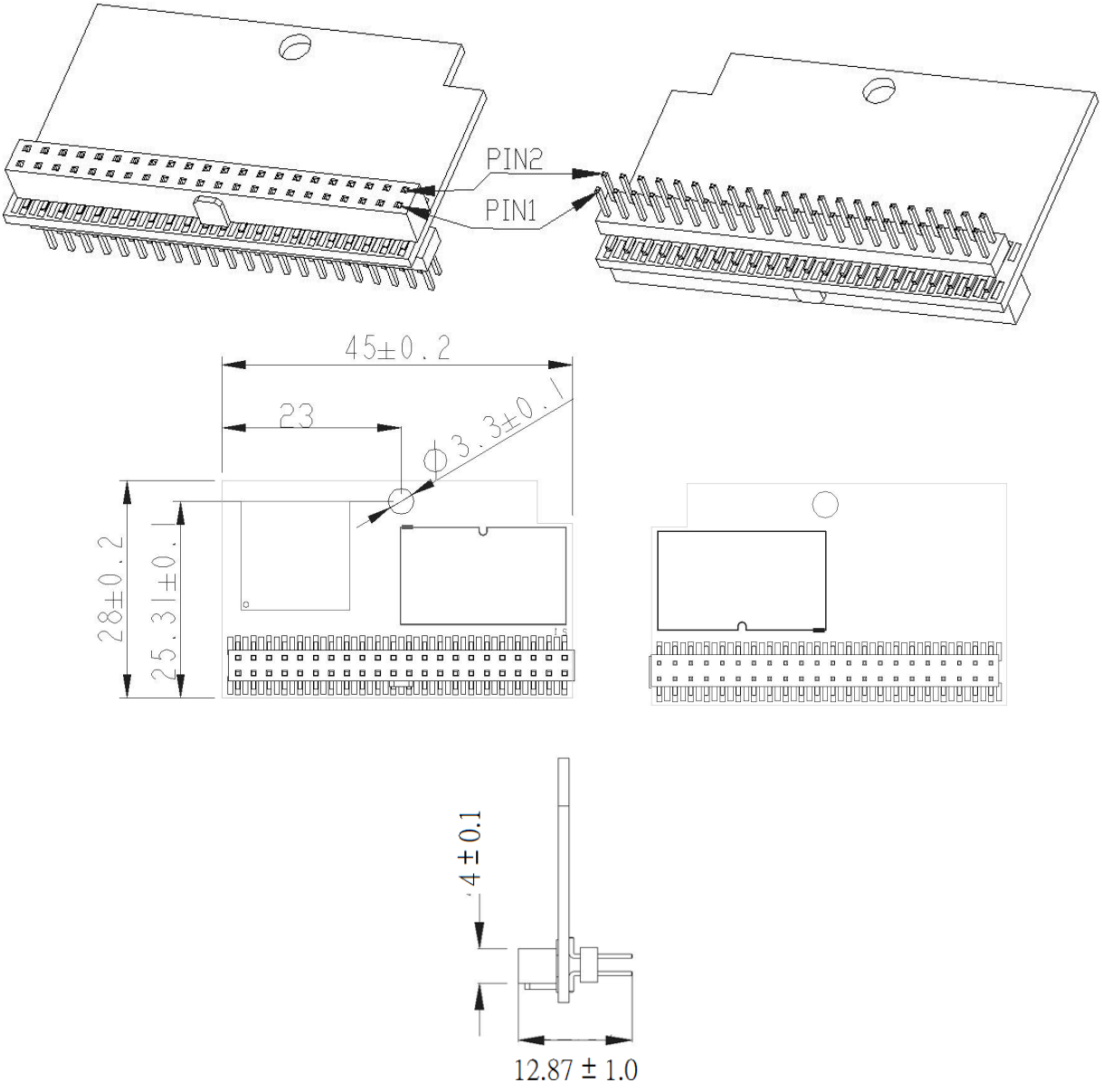
TYPE_2



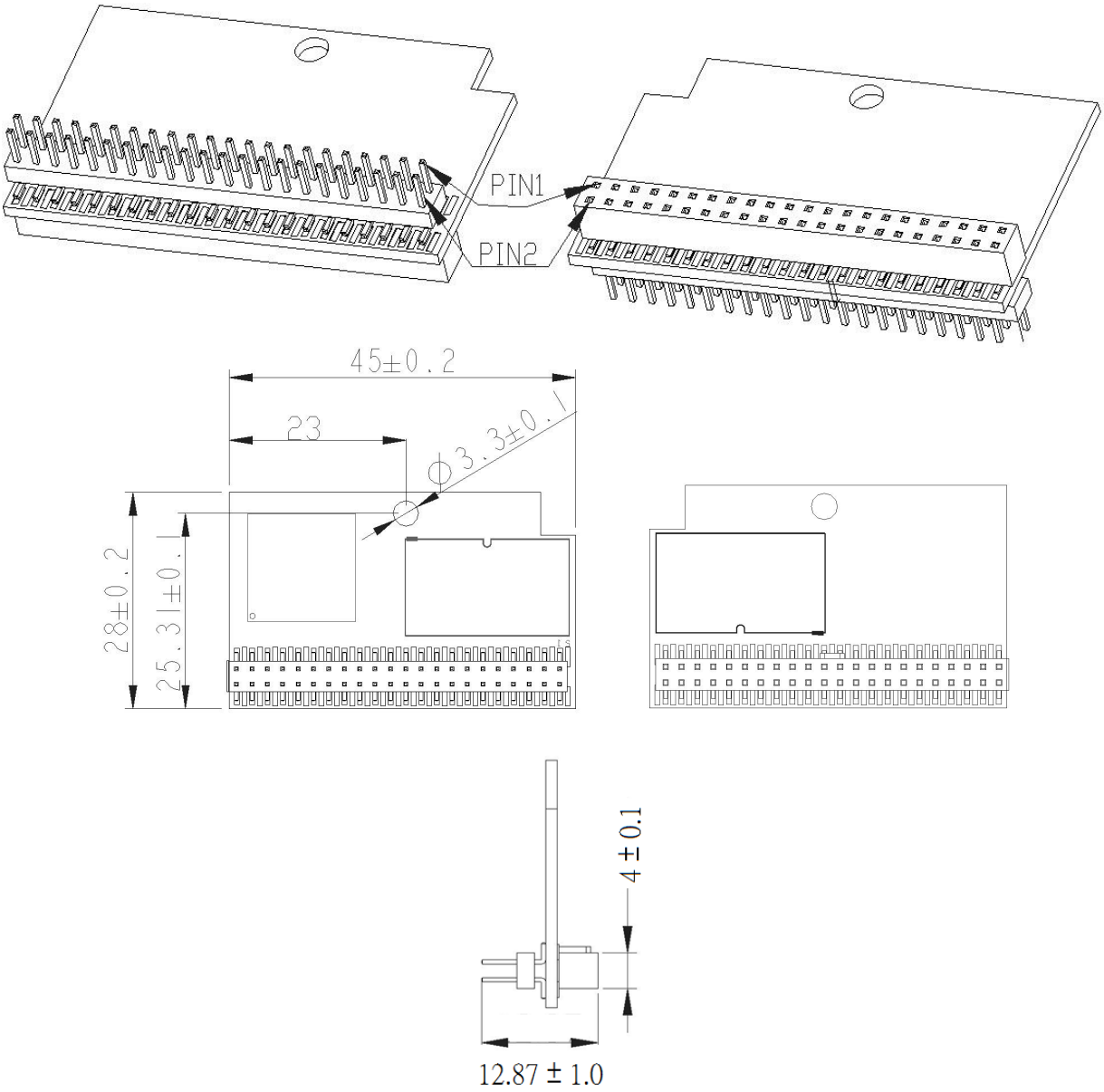




TYPE_3



TYPE_4

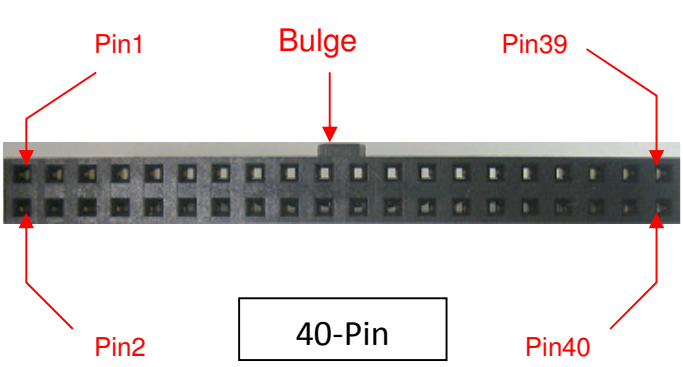


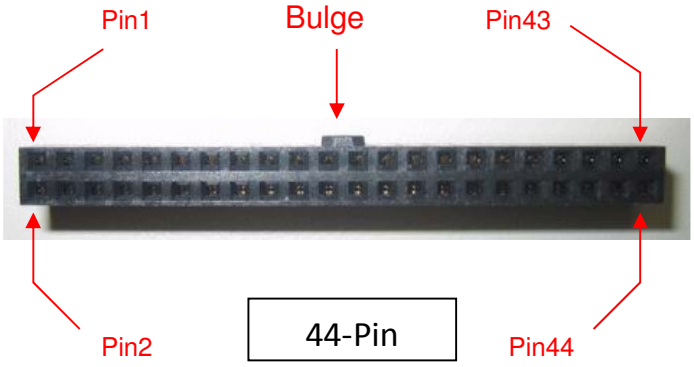
■ Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	RESET	02	GND
03	HD7	04	HD8
05	HD6	06	HD9
07	HD5	08	HD10
09	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20*	**VCC (40-PIN) / KEY (44-PIN)**
21	DMARQ	22	GND
23	HIOW	24	GND
25	HIOR	26	GND
27	IORDY	28	**NC**
29	DMACK	30	GND
31	IREQ	32	IOIS16
33	HA1	34	PDIAG
35	HA0	36	HA2
37	CE1	38	CE2
39	DASP	40	GND
41**	VCC	42**	VCC
43**	GND	44**	GND

*Note: Pin 20 is defined as VCC in the 40-Pin IDE Flash Module and KEY in the 44-Pin IDE Flash Module.
**Note: The 40-Pin IDE Flash Module does not contain Pin 41-44.

■ Pin Layout





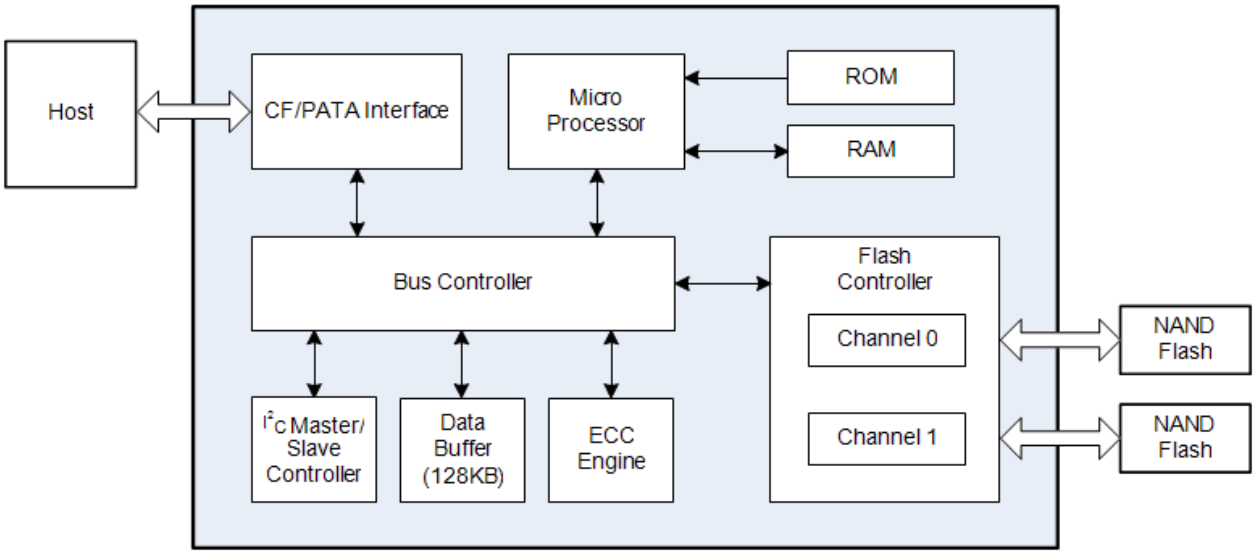
■ Pin Definition

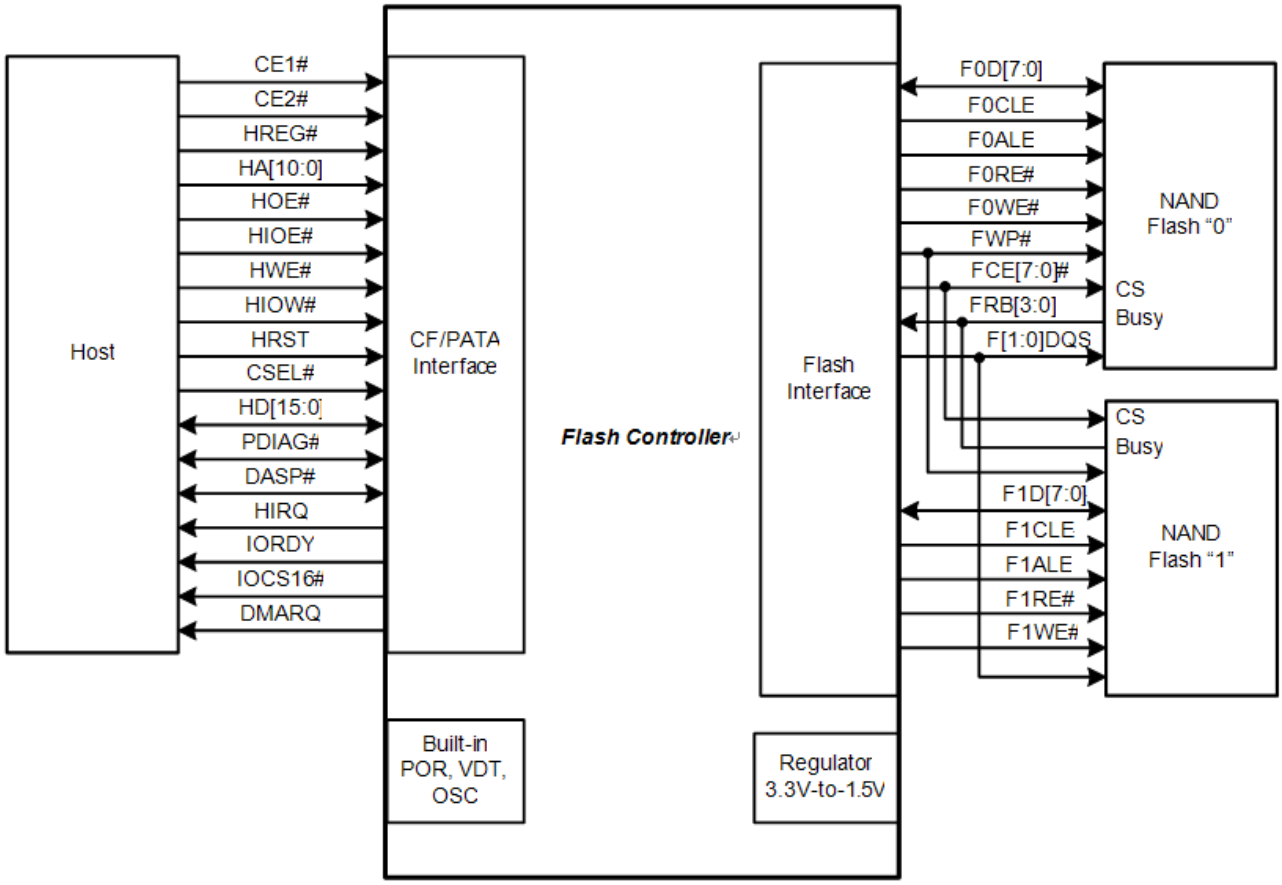
Symbol	Function
HD0 ~ HD15	Data Bus (Bi-directional)
HA0 ~ HA2	Address Bus (Input)
RESET	Device Reset (Input)
HIOR	Device I/O Read (Input)
HIOW	Device I/O Write (Input)
IOIS16	Transfer Type 8/16 bit (Output)
CE1, CE2	Chip Select (Input)
PDIAG	Pass Diagnostic (Bi-directional)
DASP	Disk Active/Slave Present (Bi-directional)
DMARQ	DMA request
DMACK	DMA acknowledge
IREQ	Interrupt Request (Output)
NC	No Connection
GND	Ground
VCC	Power Input

■ Input Power for 40-Pin IDE Flash Module

The 40-Pin IDE Flash Module offers 2 ways to get input power, either via the small power cord or through Pin 20 of the IDE connector. If Pin 20 of the IDE connector is defined as NC (No Connect), then the 40-Pin IDE Flash Module must be directly connected to your system's power supply. If Pin 20 of the IDE connector is defined as VCC, then the 40-Pin IDE Flash Module can get necessary power without use of the power cord.

■ Block Diagram





■ Reliability

Global Wear Leveling – Advanced algorithm to enhance the Wear-Leveling Efficiency

Global wear leveling ensures every block has an even erase count. By ensuring all spare blocks in the SSD's flash chips are managed in a single pool, each block can then have an even erase count. This helps to extend the lifespan of a SSD and to provide the best possible endurance.There are three main processes in global wear -leveling:

1. Record the block erase count and save this in the wear-leveling table.
2. Finds the static-block and saves this in the wear-leveling pointer.

Checks the erase count when a block is pulled from the pool of spare blocks. If the erased block count is larger than the Wear Count (WEARCNT), then the static blocks are leveraged against the over-count blocks.

StaticDataRefresh Technology – Keeping Data Healthy

Many variants may disturb the charge inside a Flash cell. These variants can be: time, read operations, undesired charge, heat, etc. Each variant would create a charge loss, which slightly influences the charge levels. In our everyday usage, more than 60% are repeated read operations, and the accumulated charge loss would eventually result in the data loss. Normally, the ECC engine corrections take place without affecting normal host operations. Over time, the number of bit errors accumulated in the read transaction exceeds the correcting capacity of the ECC engine, which results in corrupted data being sent to the host. To prevent this, the controller monitors the bit error levels during each read operation; when the number of bit errors reaches the preset threshold value, the controller automatically performs a data refresh to “restore” the correct charge levels in the cell. Implementation of StaticDataRefresh Technology reinstates the data to its original, error-free state, and hence, lengths the data’s lifespan.

EarlyRetirement – Avoiding Data Loss Due to Weak Block

The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot store charge reliably anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of “EarlyRetirement.” Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free.

Advanced Power Shield – Avoiding Data Loss during Power Failure

When a power failure takes place, the line voltage drops. When it reaches the first Logic-Freeze Threshold, the core controller is held at a steady state. Here are some implications: Firstly, it ceases the communication with the host. This prevents the host from sending in further address/instructions/data that may be corrupted. During power disturbance, the host is likely experiencing a voltage drop, so the transmission integrity cannot be guaranteed. Secondly, it stops sending the information to the Flash, which prevents the controller from corrupting the address/data being transmitted to the Flash, and corrupting the Flash contents inadvertently. Furthermore, Advanced Power Shield cuts off the connection of host power and turns off the controller to reserve most of the energy for NAND Flash to complete programming. Owing to the SLC structure, an interrupted programming may damage a paired page and cause the loss of the previously written data.

■ ATA/ATAPI Command List

Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h or 21h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h or 31h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

■ General Feature Set

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This command reads out 512 Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Identify Device Information Default Value

Word Address	Default value (Hex)	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	C837h	2	Reserved
3	00XXh	2	Default number of heads
4-5	0000h	4	Obsolete
6	XXXXh	2	Default number of sectors per track
7 - 8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10 - 19	XXXXh	20	Serial number in ASCII (Right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0000h	2	Obsolete
23 - 26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27 - 46	XXXXh	40	Model number in ASCII (Left justified). Big Endian Byte Order in Word.
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track

Word Address	Default value (Hex)	Total Bytes	Data Field Type Information
57 - 58	XXXXh	4	Current capacity in sectors (LBAs) (Word57 = LSW , Word58 = MSW)
59	0100h	2	Multiple sector setting
60 - 61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69 -79	0000h	22	Reserved
80	03FCh	2	Major version number (ATAPI-8)
81	0000h	2	Minor version number
82	7428h	2	Command sets supported 0
83	5100h	2	Command sets supported 1
84	4000h	2	Command sets supported 2
85	0000h	2	Command sets enabled 0
86	0000h	2	Command sets enabled 1
87	0000h	2	Command sets enabled 2
88	203Fh	2	Ultra DMA mode supported and selected
89	0003h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	3	Master Password Revision Code
93	604Fh 6F00h 603Fh	2	• Hardware reset result (Master only) • Hardware reset result (Slave only) • Hardware reset result (Master w/ slave present)
94 - 127	0000h	68	Reserved
128	0001h	2	Security Status
129-159	XXXXh	62	Vendor specific
160	0000h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes support
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	• CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting • 80 ns cycle in memory and I/O mode
165 - 175	0000h	22	Reserved
176 - 255	0000h	160	Reserved

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h or 21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command sets parameter to Features register and sets drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h or 31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors.

NOP (00h)

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the

Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

■ Power Management Feature Set

CHECK POWER MODE (E5h or 98h)

The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

■ Security Mode Feature Set

SECURITY SET PASSWORD (F1h)

This command sets user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content 1

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disables LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information 2

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

■ SMART Feature Set

Transcend IDE SSD supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit. Individual SMART commands are identified by the value placed in the Feature register. The table below shows these Feature register values.

SMART Feature Register Values			
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

SMART DISABLE OPERATIONS

B0h with a Feature register value of D9h.Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.

Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

B0h with a Feature register value of D2h.Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

SMART ENABL OPERATIONS

B0h with a Feature register value of D8h.Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters

SMART EXECUTE OFF-LINE IMMEDIATE

B0h with the content of the Features register equals to D4h. This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

SMART RETURN STATUS

B0h with a Feature register value of DAh. This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and the LBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

SMART Read Data

B0h with the content of the Features register equals to D0h. This command returns the Device SMART data structure to the host.

SMART DATA Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data by SMART command.

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-399	R	Reserved
400-406	F	'SMI2236'
407-511	R	Reserved

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

SMART Attributes

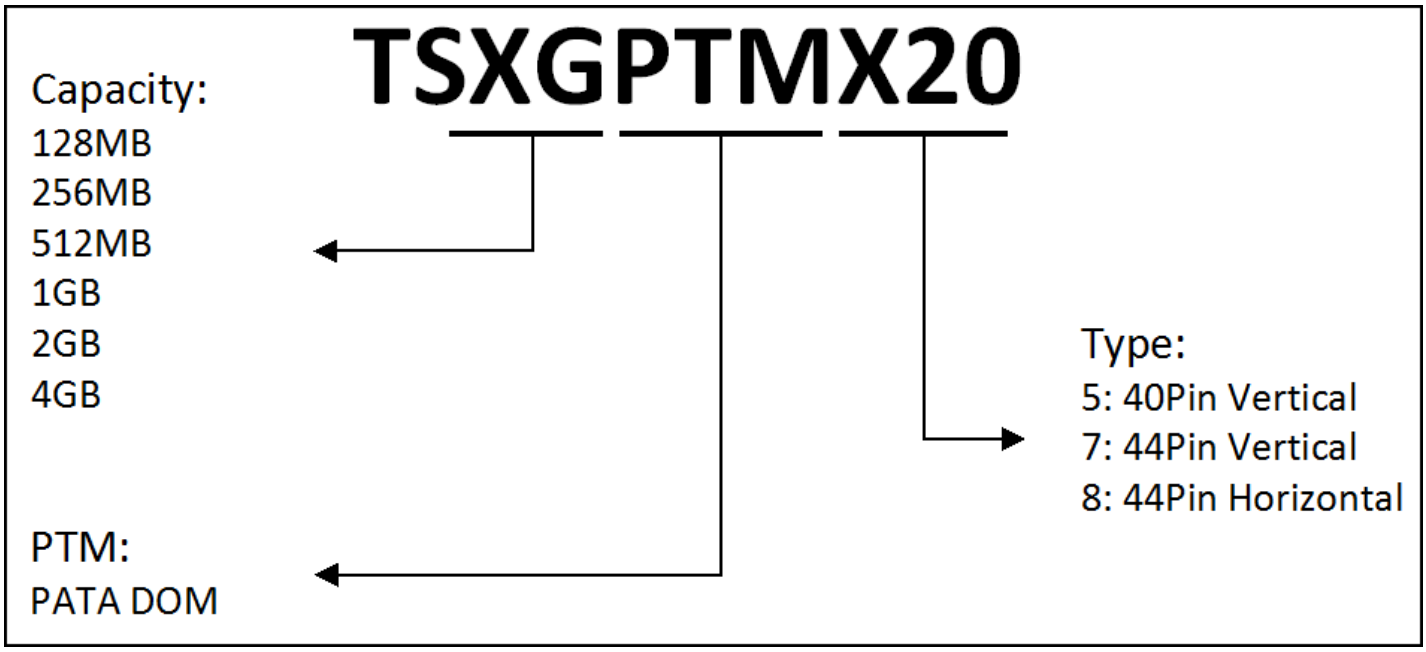
The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Attribute ID(hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	Reallocated sector count
09	LSB	MSB	00	00	00	00	Reserved
0C	LSB	MSB	00	00	00	00	Power cycle count
A0	LSB	~	~	MSB	00	00	Uncorrectable sector count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare block
A2	LSB	MSB	00	00	00	00	Number of child pair
A3	LSB	MSB	00	00	00	00	Number of initial invalid block
A4	LSB	~	~	MSB	00	00	Total erase count
A5	LSB	~	~	MSB	00	00	Maximum erase count
A6	LSB	~	~	MSB	00	00	Minimum erase count
A7	LSB	~	~	MSB	00	00	Average erase count
C0	LSB	~	~	MSB	00	00	Power-off retract count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB	~	~	MSB	00	00	Hardware ECC recovered
C4	LSB	~	~	MSB	00	00	Reallocation event count
C6	LSB	~	~	MSB	00	00	Reserved
C7	LSB	MSB	00	00	00	00	Ultra DMA CRC error count
F1	LSB	~	~	MSB	00	00	Total LBA written (each write unit=32MB)
F2	LSB	~	~	MSB	00	00	Total LBA read (each write unit=32MB)

■ Host Protected Area Feature Set

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The optional Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured.

■ Ordering Information



The technical information above is based on commercial standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

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TAIWAN
No.70, XingZhong Rd., NeiHu Dist., Taipei, Taiwan, R.O.C
TEL +886-2-2792-8000
Fax +886-2-2793-2222
E-mail: sales-tw@transcend-info.com
http://tw.transcend-info.com

USA
Los Angeles:
E-mail:sales-us@transcend-info.com
Maryland:
E-mail:sales-us@transcend-info.com
Florida:
E-mail:sales-us@transcend-info.com
Silicon Valley:
E-mail:sales-us@transcend-info.com
http://www.transcend-info.com

CHINA
Shanghai:
E-mail: sales-cn@transcendchina.com
Beijing:
E-mail: sales-cn@transcendchina.com
Shenzhen:
E-mail:sales-cn@transcendchina.com
http://cn.transcend-info.com

GERMANY
E-mail:vertrieb-de@transcend-info.com
http://de.transcend-info.com

HONG KONG
E-mail: sales-hk@transcend-info.com
http://hk.transcend-info.com

JAPAN
E-mail: sales-jp@transcend-info.com
http://jp.transcend-info.com

THE NETHERLANDS
E-mail: sales-nl@transcend-info.com
http://nl.transcend-info.com

United Kingdom
E-mail: sales-uk@transcend-info.com
http://uk.transcend-info.com

KOREA
E-mail:sales-kr@transcend-info.com
http://kr.transcend-info.com

Revision History

Version	Date	Modification Content	Modified Page
V1.0	2015/02/24	Initial beta release	
V2.0	2015/08/12	1. Combine datasheet of PTM series product 2. Update ID table and SMART Attributes table	